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APPLICATION NUMBER: ***60/550,358***
FILING DATE: ***March 04, 2004***
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This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

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60/550358
030404

INVENTOR(S)		
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Additional inventors are being named on the 1 *separately numbered sheet attached hereto*

TITLE OF THE INVENTION (500 characters max)

Low Cost Digital Controller for a Switching DC-DC Converter with Improved Voltage Regulation

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

[X] Customer Number: 39602

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ENCLOSED APPLICATION PARTS *(check all that apply)*

[X] Specification *Number of Pages* 14
[ ] Drawing(s) *Number of Sheets* ______
[ ] Application Data Sheet. See 37 CFR 1.76
[ ] CD(s), Number ______
[ ] Other (specify) ______

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

[ ] Applicant claims small entity status. See 37 CFR 1.27.
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The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government

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[Page 1 of 2]

Respectfully submitted,

SIGNATURE ______

TYPED or PRINTED NAME Daniel J. Noblitt

TELEPHONE 480.994.9859

Date 04 Mar 2004

REGISTRATION NO. 35969
(if appropriate)

Docket Number: AZEN.0250/M4-054

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Docket Number **AZEN.0250/M4-054**

INVENTOR(S) /APPLICANT(S)		
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FEE TRANSMITTAL for FY 2004

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☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 160.00

Complete if Known	
Application Number	NYA
Filing Date	04 Mar 2004
First Named Inventor	Islam, et al.
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Deposit Account Number: 50-2993

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	160

SUBTOTAL (1) ($) 160.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims	-20**=		x		=	
Independent Claims	- 3**=		x		=	
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)160.00

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) ____________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)160.00

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Daniel J. Noblitt	*Registration No. (Attorney/Agent)*	35969	*Telephone*	480.994.9859
Signature	[signature]			*Date*	04 Mar 2004

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Copy of Lab Hand Book

1111 — $d = d - sd$

——— V_h

0111 — $d = d - 1$

——— V_{mh}

0011 — $d = d$

——— V_{ml}

0001 — $d = d + 1$

0000 ——— V_l

$d = d + sd$

sd = Coarse change

D5					D0	
1	1	1	1	1	1	← L63
1	1	1	1	1	0	
			1	0	1	
			1	0	0	
			0	1	1	
			0	1	0	
			0	0	1	
			0	0	0	

→ Changes 1
→ Change by 2
→ by 4
→ Change by 8
→ by 16
→ by 32

D_0 Change : 1.5625 mv effect
D_1 " : 3.125 mV "
D_2 " : 6.25 mV "
D_3 " : 12.5 mV "
D_4 " : 25 mV "
D_5 " : 50 mV "

11/03/03

* Shield A/D Board
* Design the Board and Write a code for 4-level Control.

discontinuous Mode ($d = d - 1$)

——— Vhigh (1.85)

dither_down (dither duty)

——— Vm-high (1.81)

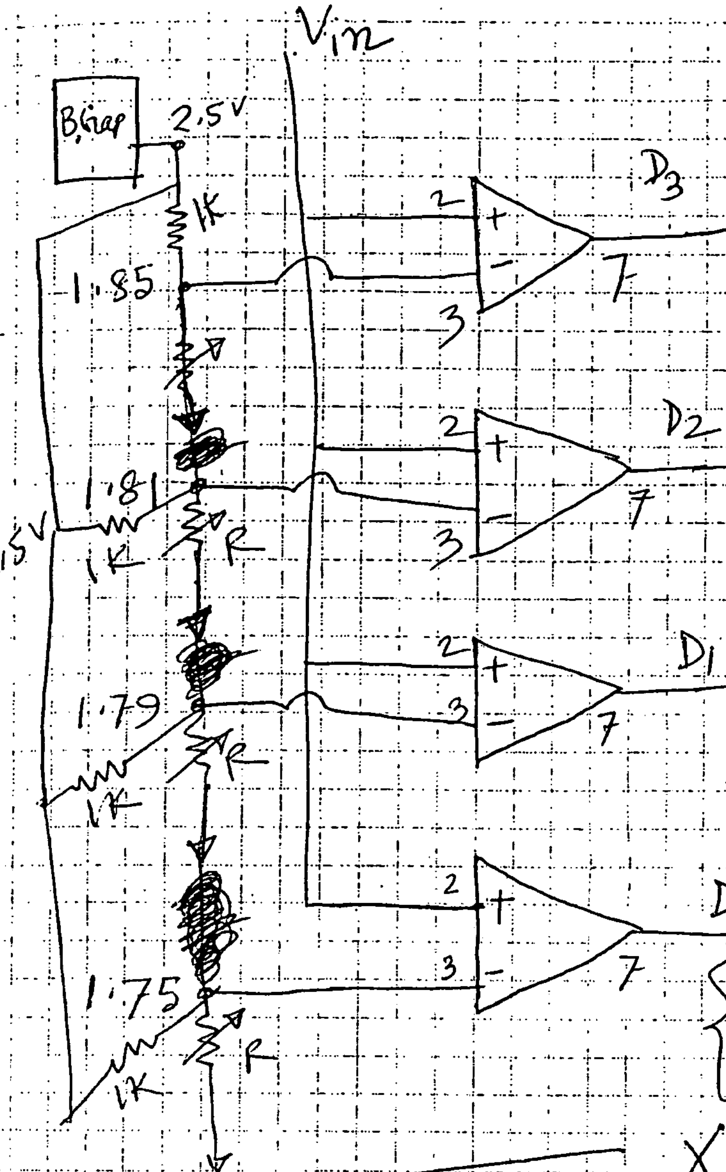
Continuous ($d = d$) - - - - (Exact o/p 1.8V)

——— Vm-low (1.79)

dither_up (dither duty)

——— Vlow (1.75)

ramp up ($d = d + 1$)



{ disc. mode (Switch OFF until D_3 becomes 0)

{ Dither down (dither duty down to drive V_o to continuous state)

{ Continuous State (duty is ~~same~~ same in this state, no d change)

{ Dither up (dither duty up to drive V_o to Continuous State)

{ Ramp mode (Switch ON until D_0 becomes 1)

X

* Need −1 V to +1 Volt (level Shift for 10 bit ADI A/D)

$$V_o = -\frac{R_2}{R_1} V_x + V_i \left(\frac{R_4}{R_3+R_4}\right)\left(1+\frac{R_2}{R_1}\right)$$

So, $\frac{R_2}{R_1} = 1$ @, $V_i = 0$, $V_o = -1$

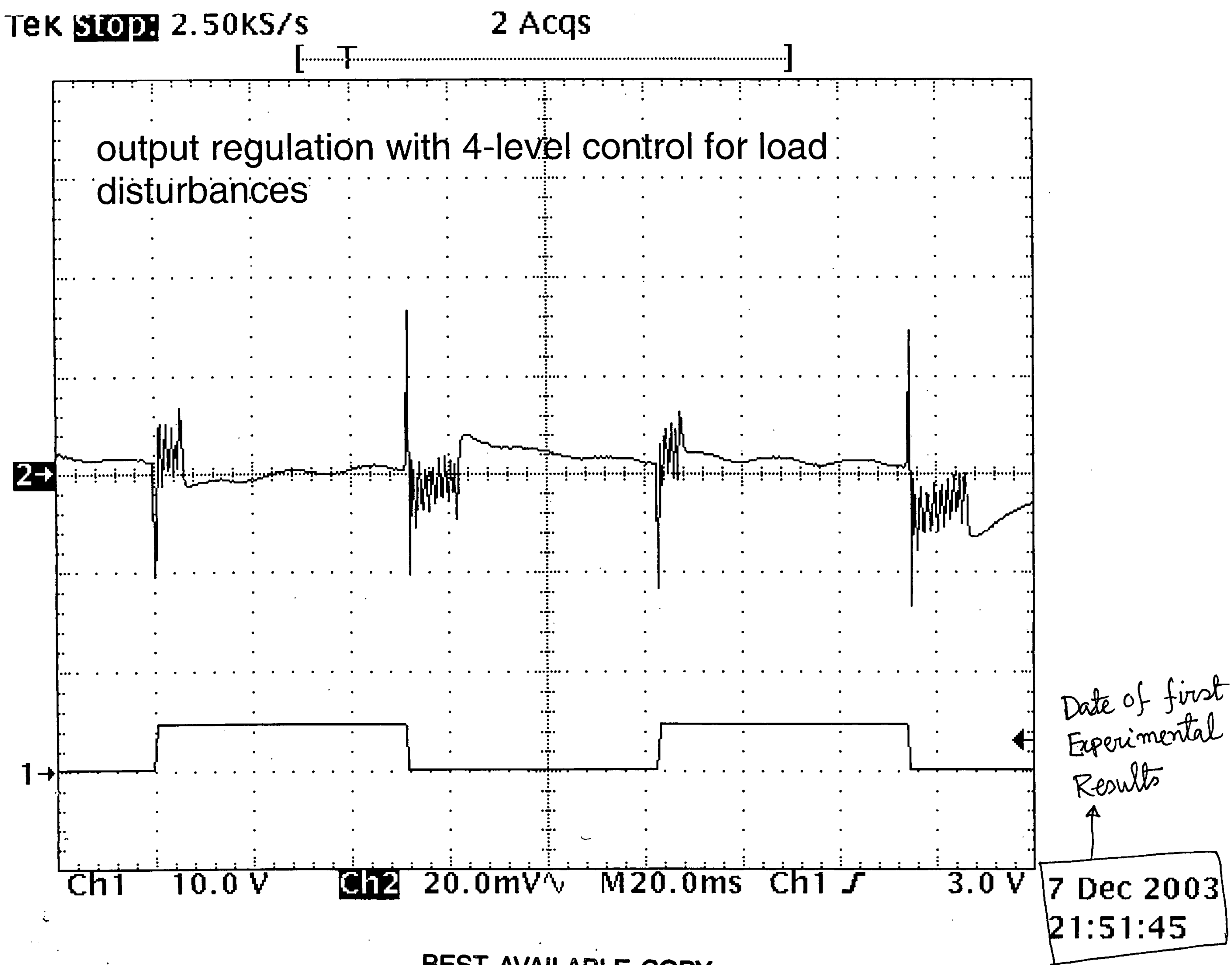
So, make, $V_x = 1\,V$

@ $V_i = 2V$, $V_o = +1$,

$$\frac{R_4}{R_3+R_4} = 0.5$$

$0.5R_4 = 0.5R_3$

$\boxed{R_4 = R_3}$ $\boxed{R_1 = R_2}$, $\boxed{V_x = 1\,V}$



Date of first Experimental Results

A Low Cost Digital Controller for a Switching DC-DC Converter with Improved Voltage Regulation

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Department of Electrical Engineering
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Abstract

A new control algorithm with improved regulation is presented for a switching dc buck converter. The controller is realized with Hardware Description Language (HDL) and can be implemented in any process. The controller uses four decision levels and takes the advantages of the pulse frequency modulation (PFM) and the pulse width modulation (PWM) for better performance. It also uses dithering for improved regulation. The controller is prototyped on a Field Programmable gate Array (FPGA) and experimental results show good performance over input and load disturbances. Most of all, the controller does not require high resolution analog to digital converter for signal processing and also does not require fast digital clock for improved regulation. This controller has significant potential to be widely used in industrial applications where cost and design time are of great concern.

1. Introduction:

The output voltage regulation for a dc dc converter has traditionally been accomplished using analog circuits that are custom designed for particular applications [1]. While this approach has been commercially successful over many years, it does lead to relatively long design, layout and testing times. However, a digital controller can be quickly designed with high-level language and automatically laid out using appropriate software. This automated process dramatically decreases the length of the design cycle. Moreover, digital controllers are flexible and allow the implementation of more functional control schemes [2-5]. Digital circuits are potentially less susceptible to noise and parameter variations. The disadvantage with digital control is generally inferior voltage regulation. Other issues hampering the applications of digital controllers are cost/performance, availability, and/or ease of use [3]. Available DSP systems or micro-controllers require a high resolution Analog to digital converter (A/D), which in turn increases the word length for the DSP calculation, area and cost. In [3] the conventional flash A/D has been replaced with a time delay A/D and the Digital Pulse-Width Modulator (DPWM) has been designed with hybrid delay-line/counter approach [3,6]. The design is very satisfactory but is not process independent. Here the A/D and the DPWM depend on process parameters to get the expected delay and requires a new custom design for new processes. However, it is preferable to design a digital controller that is modeled in HDL and can be transferred from one process to another without any changes in the algorithm. The design also needs to be small in area and without having much complexity in order to be competitive with traditional analog controllers.

In this report, a digital controller is presented that uses only four decision levels to achieve an improved regulation and better performance. A block diagram of buck converter with four comparators is shown in Fig. 1. The basic algorithm is presented in section 2 and is realized with verilog-HDL. The experimental results for various disturbances are presented in section 3.

The results show good performance considering complexity, area and output regulation. The controller is entirely digital making it less sensitive to process variation and it can be implemented on any process.

2. Background Theory:

Due to its flexibility and rapidness in nature, digital controllers are becoming popular day by day in the area of power management. Recently, a few companies have introduced dc dc converters with digital controllers. A good example is Philips TEA1206 [7]. In [8] a digital controller has been proposed that uses two decision levels and takes the advantages of two different types of control schemes- pulse width modulation (PWM) and pulse frequency modulation (PFM) control. The problem with this controller is that if we reduce the voltage separation between the two levels then the instability arises. A good choice is to take at least ±2% of output voltage spreading on both sides of the expected output voltage level [7]. Another disadvantage of 2-level control is that the regulation is poor as the controller lacks information while the output voltage is in between the window i.e. between the two reference levels.

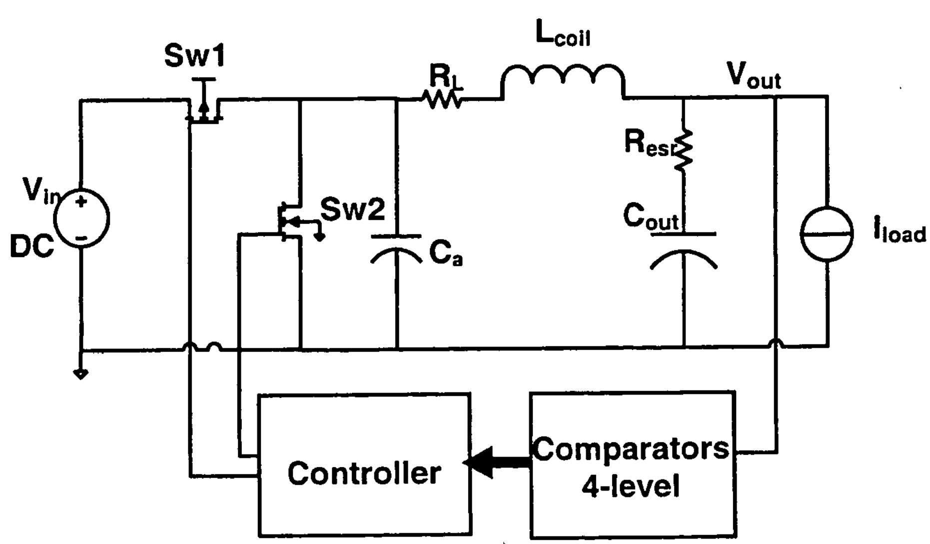

Fig. 1. Buck Converter with Digital Controller

To take advantage of the window concept and also overcome the regulation problem, a 4-level controller is proposed here. This controller has 2-internal levels (Vm-high, Vm-low) which are used for improved regulation and 2-external levels (Vhigh,Vlow) that are used for fast recovery. The state diagram for the 4-level digital controller is shown in Fig. 2. Two comparators with decision levels ±2% above and below the output voltage determine the states for fast recovery. These states are discontinuous state and ramp-up states. The 2-internal levels are set from the Effective Series Resistance (ESR) of output capacitor or the maximum possible ripple voltage. These two internal levels create three more states realized here as dither-up, dither-down and continuous states.

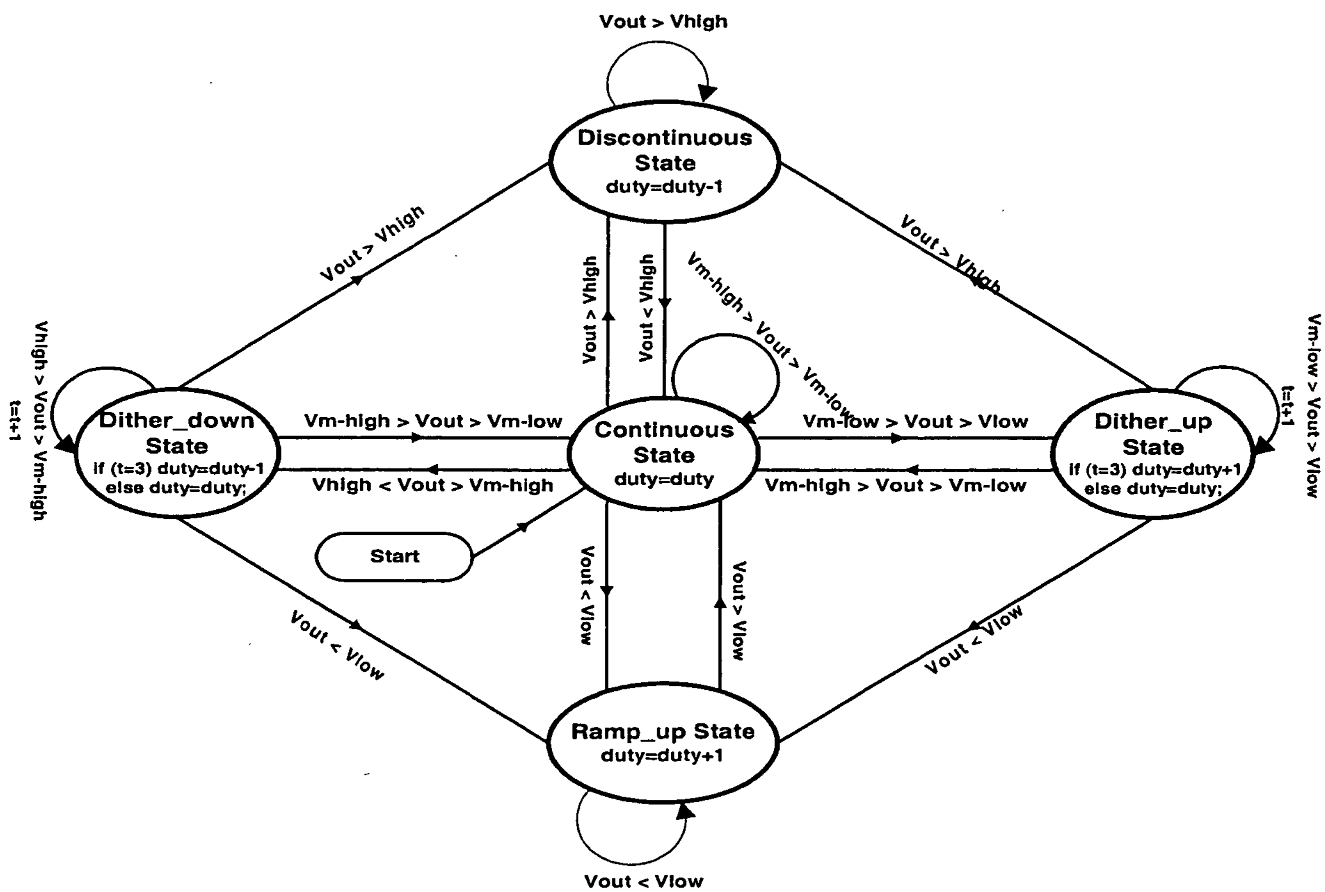

Fig. 2. State Diagram for a 4-level Controller

If the output voltage decreases below Vlow, the finite state machine moves into ramp up mode. This usually is the result of a sudden increase in the required load current. The quickest way to return to the desired output voltage range is to hold the power switch (sw1 in Fig. 1) on. The current through the inductor linearly rises providing more current to the load and raising the output voltage. At the end of each digital clock period, the output is monitored to determine if the output has risen back to the desired range. When it does, the finite state machine returns to the continuous state, but with a slightly larger duty cycle. If the duty cycle is still too low, the output voltage will again fall below Vlow and the cycle repeats further increasing the duty cycle.

Since the controller is digital, the duty cycle can only be set at time increments corresponding to digital clock. For example, with a 10MHz digital clock (100ns period) and a 100KHz switching clock (10us period), the duty cycle can only be set at increments of 0.01(100ns/10us). This results in a coarse setting of the output voltage. A simple way to achieve high duty resolution is to increase the digital clock frequency. A digital clock frequency of 1GHz with a switching frequency of 100KHz allows the duty cycle to be set to 1 part in 10,000. That is, there are 10000 digital clock periods in 1 switching cycle. However, this would lead to excessive power consumption in the digital circuitry and require an expensive deep sub-micron process. An alternative approach to achieve high resolution using low digital clock is known as dithering. The idea behind the digital dither is to vary the duty cycle by a Least Significant Bit (LSB) over a few switching periods, so that the average duty cycle has a value between two adjacent duty cycle levels. The output LC filter performs the averaging action required for dithering [9]. As an example, a duty cycle of 0.3633 could be achieved with a dithering over 4 cycles with subsequent duty cycles of 0.36, 0.36, 0.37 and 0.36.To achieve this high resolution in duty cycle, dithering was done in our controller as long as the output stays in dither_up or dither_down states. In dither_up states the duty is increased by one step after subsequent wait cycles to drive

the output voltage into the desired internal window region. Similarly, in dither_down state the duty is decreased by one step after subsequent period to achieve the desired regulation. If the output voltage is in between the internal window, the controller works in continuous state without any changes into the duty cycle.

If the output voltage exceeds Vhigh, the finite state machine moves into the discontinuous state. This usually is the result of a sudden decrease in the required load current. The quickest way to return to the desired output voltage range without wasting energy stored on the output capacitor is to simply allow the load to draw all its current from the output capacitor. The power switch (sw1 in Fig. 1) is kept off preventing any additional current flowing through the inductor to the load. At the end of each digital clock period, the output is monitored to determine if the output has fallen back into the desired range. When it does, the finite state machine returns to the continuous state but with a slightly decreased duty cycle. If the duty cycle is still too high providing too much load current, the load voltage will again rise above Vhigh and the cycle repeats further decreasing the duty cycle.

From the above discussion, it is obvious that the discontinuous and ramp-up operation ensures fast response in case any disturbance occurs and the dithering ensures better regulation when the load is constant or the change is small.

3. Experimental Results:

A 2-level and 4-level control scheme has been implemented on a Virtex™ XCV300-6PQ240C device. The 2-level control has two decision levels as Vhigh and Vlow and operates in three states as discontinuos, continuous and ramp up. The state diagram of 2-level control is shown in Fig. 3. The buck converter is implemented on a Printed Circuit Board (PCB) with standard components. The digital clock runs at 50 MHz and the switching clock is at 100KHz. As can be seen in Fig. 4 and Fig. 6, the output regulation for 2-level controller is very poor for

load and input disturbances. The regulation is around 70mv for a load disturbance of 200mA to 600mA at a rate of 100Hz. For input disturbances from 3V to 6V at a rate of 100Hz, the regulation in 2-level control is about 80mv. The reason for this poor regulation is the lack of information in between the two reference window. With the same load and input disturbances, the 4 level controller gives much better regulation than the 2-level as can be seen in Fig. 5 and Fig. 7 respectively. It should be noted that the improvement in regulation in 4-level control comes with only two additional comparators. The numbers of slices used for implementing the 2-level and 4-level controller are 67 and 103 respectively, which represents about 2% and 3% of resources on a XCV300 device. For comparison purposes a DSP implementation of the Type-3 analog compensator was also performed using Xilinx System Generator. This implementation uses 16*16 multiplier to realize the digital filter and requires about 48% chip area on the same device. So, it can be said that the 4-level controller is a very good choice for improved regulation considering simplicity, area and performance.

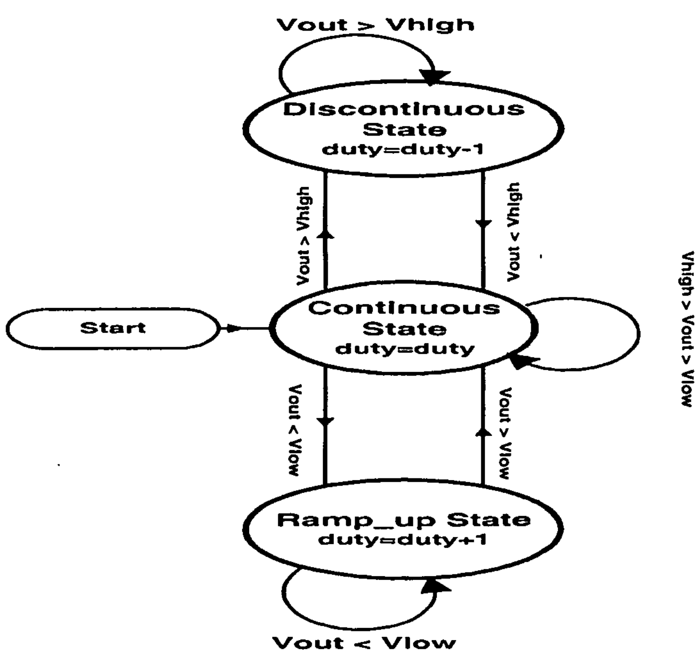

Fig. 3. State Diagram for a 2-level Controller

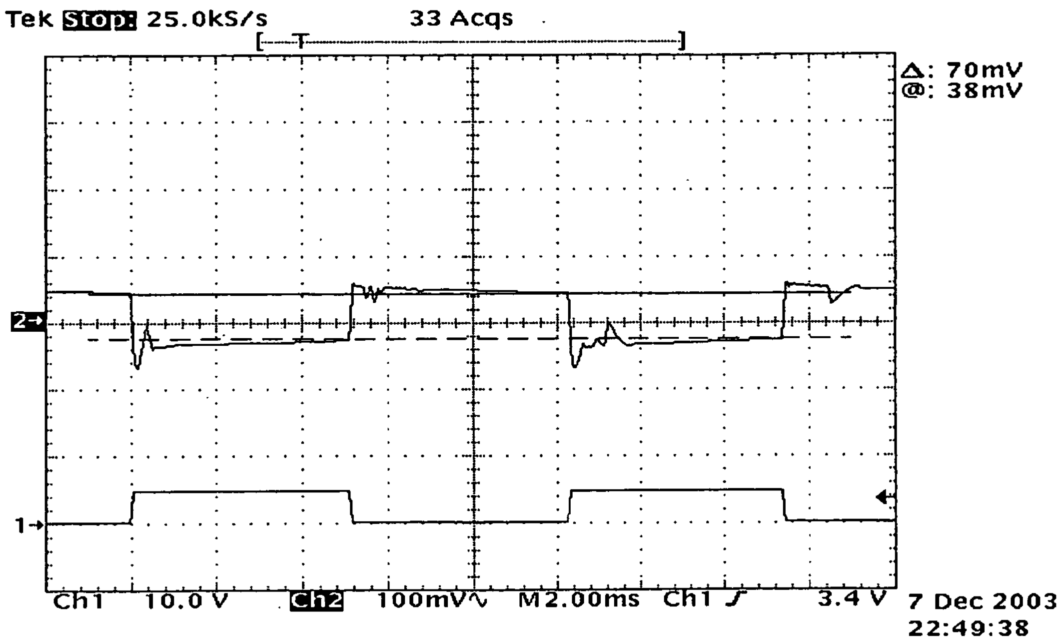

Fig. 4. Output regulation for 2-level controller with load disturbances

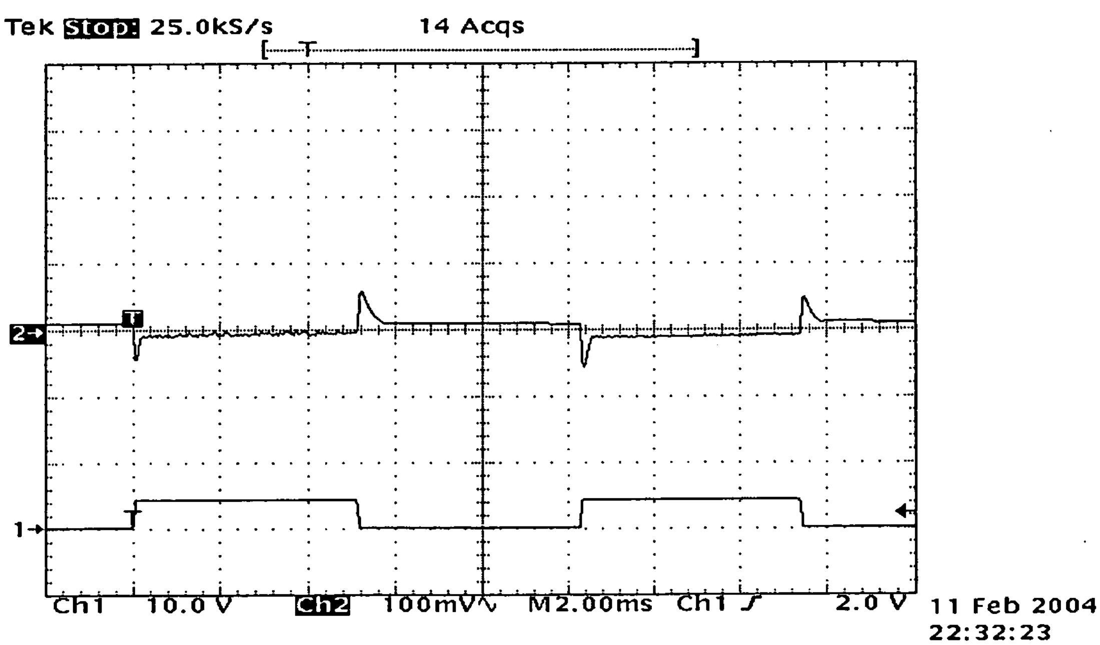

Fig. 5. Output regulation for 4-level controller with load disturbances

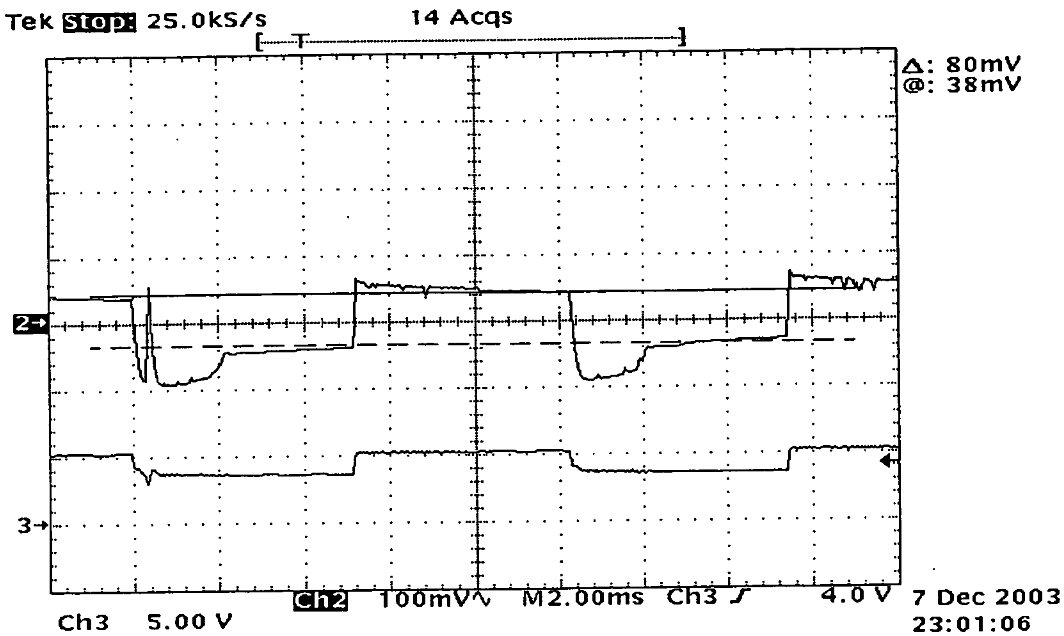

Fig. 6. Output regulation for 2-level controller with input disturbances

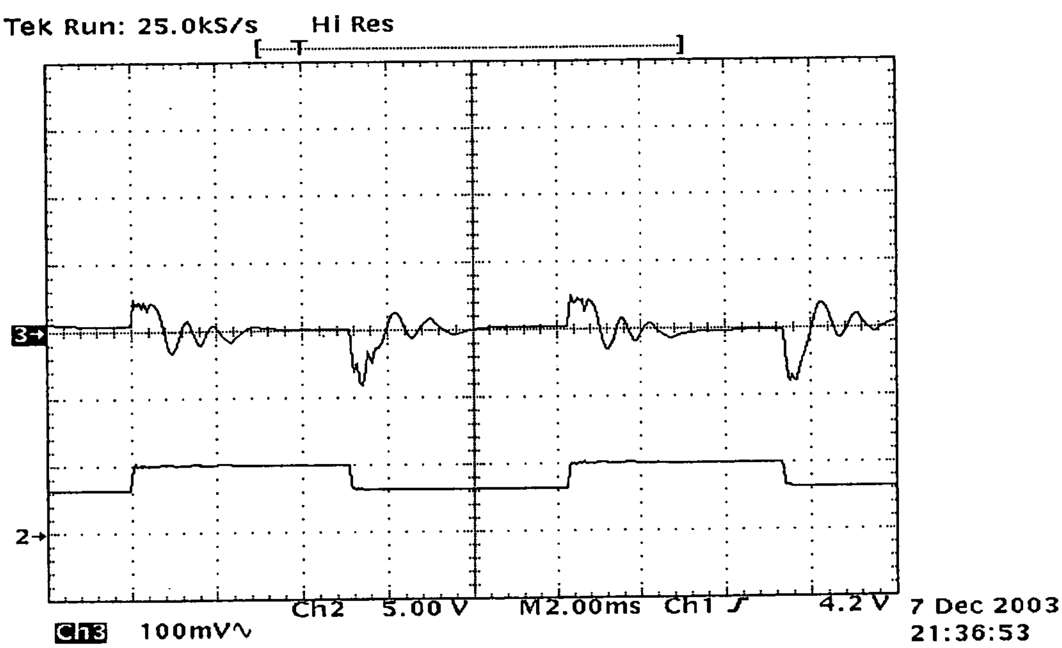

Fig. 7. Output regulation for 4-level controller with input disturbances

4. Conclusion:

A four level controller is presented with state diagram and experimental results. The controller shows good performance for input and load disturbances over its 2-level counterpart. Replacing the high resolution A/D, required for most DSP calculation, with comparators is a significant improvement considering area, cost and complexity. Also the pulse frequency operation described in ramp up and discontinuous mode provides fast recovery for any disturbances. The extra window allows the controller to work in dithering state, which eventually improves the regulation. Moreover, the algorithm is realized in verilog-HDL and implemented on a Virtex™ FPGA device. The controller uses logical comparison to make any decision and avoids any complexity related to multiplication, addition etc. to implement the algorithm. So this control technique can be a potential candidate to be widely used in commercial applications due to its simplicity, performance and rapid transformation from process to process.

References

[1] R. R. Boudreaux, R. M. Nelms, and John Y. Hung, "Simulation and Modeling of a DC-DC Converter by an 8-bit Microcontroller," IEEE Applied Power Electronics Conference, 1997, vol. 2, pp. 963-969.

[2] Y. Duan, H. Jin, "Digital Controller Design for Switch Mode Power Converters," IEEE Applied Power Electronics Conference, 1999, vol. 2, pp. 967-973.

[3] B. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-Frequency Digital Controller IC for DC/DC Converters," IEEE Applied Power Electronics Conference, 2002, vol. 1, pp. 374-380.

[4] J. Xiao, A. V. Peterchev, S. R. Sanders, "Architecture and IC Implementation of a digital VRM controller," IEEE Power Electronics Specialists Conference, 2001, vol. 1, pp. 38-47.

[5] A. M. Schultz, S. B. Leeb, A. H. Mitwali, D. K. Jackson, G. C. Verghese, " A multirate digital controller for an electric vehicle battery charger," IEEE Power Electronics Specialists Conference, 1996, vol. 2, pp. 1919-1925.

[6] A. P. Dancy, R. Amirtharajah, A. P. Chandrakasan, "High efficiency multiple output DC-DC conversion for low-voltage systems," IEEE Trans. On VLSI Systems, vol. 8, No. 3, June 2000.

[7] TEA1206 Product Datasheet
"Available: http://www.semiconductors.philips.com/pip/TEA1206.html"

[8] F. J. Sluijs, C.M. Hart, D.W.J. Groeneveld, S. Haag, "Integrated DC/DC converter with digital controller," International Symposium on Low Power Electronics and Design, 1998, pp. 88-90.

[9] A. V. Peterchev,and S. R. Sanders, "Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters," IEEE Applied Power Electronics Conference, 2001, vol. 1, pp. 465-471.